

UNITED STATES PATENT APPLICATION

FOR

A METHOD AND DEVICE FOR IMPROVED
SALICIDE RESISTANCE ON POLYSILICON GATES

INVENTORS:

Chia-Hong Jan
Julie A. Tsai
Simon Yang
Tahir Ghani
Kevin A. Whitehill
Steven J. Keating
Alan Myers

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CALIFORNIA 90025
(408) 720-8598

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**A METHOD AND DEVICE FOR IMPROVED
SALICIDE RESISTANCE ON POLYSILICON GATES**

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FIELD OF THE INVENTION

The present invention relates to the field of semiconductor devices. More
10 particularly, the present invention relates to a method and device for improved
resistance on gate electrodes. Specifically, the present invention relates to a
method and device for improved salicide resistance on polysilicon gates.

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BACKGROUND OF THE INVENTION

Transistors are commonly used in semiconductor circuitry to control
current flow. For example, a transistor can be used as a switching mechanism to
allow the flow of current between a source and a drain region in a circuit when a
20 certain threshold voltage is met. Transistors generally include a gate electrode
that allows or prevents the flow of current in the transistor based on applied
voltage.

Figure 1a shows a cross-sectional view of a conventional gate electrode
25 100 formed on a substrate 110, the underlying structure of which is not shown. It
should be noted that the figures are merely illustrative and have been simplified
for clarity purposes. A thin insulative layer 120 is formed on the substrate 110 to
act as a barrier between the substrate 110 and the conductive portions of the gate
electrode 100. An example of an insulative layer 120 can be an oxide layer, such
30 as silicon dioxide (SiO_2). Formed on the insulative layer 120 is a gate layer 130.
An example of a gate layer 130 can be a polysilicon layer. Formed on the gate
layer 130 is a conductive layer 160. An example of a conductive layer 160 can be
a polycide layer, such as titanium salicide (TiSi_2). When a threshold voltage is
applied to the gate layer 130 by the conductive layer 160, current will flow
35 through the gate layer 130. Often insulative spacers 140 and 150 are formed to
each side of the gate layer 130 to prevent transfer of current between the gate
layer 130 and surrounding structures in the semiconductor.

5 In semiconductor circuit design, frequently, gate electrodes are designed
in long continuous lines on the semiconductor substrate to efficiently provide
current to several transistors in a circuit. Currently, improved semiconductor
transistor performance is being achieved through device scaling in which the
gate layer widths are being reduced from .20 μm to .15 μm and below (sub-.15
10 μm). As the gate layer width dimensions decrease, so do the conductive layer
line widths formed above them.

When the gate layer widths decrease below .20 μm , current process
techniques produce conductive lines with sharply increasing resistance. This is
15 detrimental to the efficiency of the semiconductor, as higher resistance decreases
the speed of the semiconductor circuitry. Additionally, process yields drop due
to defective conductive line formation reducing manufacturing output. These
problems have been particularly noted in current fabrication processes where
titanium salicide (TiSi_2) is formed as the conductive layer in a polysilicon gate.
20

Figure 1b illustrates a cross-sectional view of a conventional gate electrode
100 formed on a substrate 110, the underlying structure of which is not shown.
An example of a gate electrode 100 can be a polysilicon gate electrode. Formed
on the substrate 110 is an insulative layer 120. An example of an insulative layer
25 120 can be an oxide. Formed on the insulative layer 120 is a conductive gate
layer 130. An example of a gate layer 130 is a polysilicon layer. Formed on the
gate layer 130 is a conductive layer 160. An example of a conductive layer 160
can be a polycide, such as titanium salicide. Insulative spacers 140 and 150 are
formed adjacent to the gate layer 130 and conductive layer 160 to prevent current
30 flow between the gate layer 100 and surrounding structures.

During formation of the conductive layer 160, components from
underlying gate layer 130 often out diffuse into a reactant layer that is used to
form the conductive layer 160. For example, silicon components of an
35 underlying gate layer 130 may out diffuse into the conductive layer 160. This out
diffusion results in a conductive layer 160 wider than the gate layer 130. When

5 the gate layer 100 width is decreased below .20 μ m, the conductive layer 160 becomes stressed by its enclosure between the side walls of the spacers 140. This results in increased resistance in the conductive layer 160. Increased resistance in the conductive layer directly impacts the quality of the semiconductor circuit. The circuit becomes inefficient and circuit failure or device failure may occur.

10

Another result of decreasing the gate line widths below .20 μ m is a decrease in process yields. This is due to non-formation of the conductive layer. This is attributed to the reduced reaction area, or nucleation sites, available at such small dimensions. The reduced dimensions of the gate layer reduces 15 nucleation sites on which the conductive layer can form during processing. Using current process techniques, if sufficient nucleation sites are not provided, the conductive layer often won't form. This directly impacts the semiconductor manufacturer by reducing output.

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Based on the above described problems, it would be desirable to have a method and/or device which will improve the polycide resistance in polysilicon gate widths below .20 μ m.

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BRIEF SUMMARY OF THE INVENTION

The present invention provides a method and a device which improves polycide resistance in gate electrode widths below .20 μm . The invention
10 provides several embodiments one embodiment of which is described below.

In one embodiment of the present invention there is provided a gate electrode comprising a thin insulative layer. A gate layer is formed on the thin insulative layer. A conductive layer is formed on the gate layer. Thick first
15 spacers are formed adjacent to opposite sides of the gate layer. Thick second spacers are formed adjacent to the thick first spacers. The thick first spacers are recessed to create an open space between the gate layer and thick second spacers.

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5 BRIEF DISCUSSION OF THE SEVERAL VIEWS OF THE DRAWINGS

For fuller understanding of the present invention, reference is made to the accompanying drawings in the following detailed description of the invention.

In the drawings:

10

Figure 1(a) is a cross-sectional illustration of a conventional gate electrode in the prior art depicting a non-stressed conductive layer.

15 Figure 1(b) is a cross-sectional illustration of a conventional gate electrode in the prior art depicting a stressed conductive layer.

Figures 2 (a) - (h) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and recessed thick inner spacers and non-recessed thick outer spacers.

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Figures 3 (a) - (i) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and recessed thin inner spacers and recessed thick outer spacers.

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Figures 4 (a) - (i) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and non-recessed thin inner spacers and partially recessed outer spacers.

30

Figures 5 (a) - (m) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and two spacer stacks. The outermost spacer stack having recessed thin inner spacers and recessed thick outer spacers. The inner spacer stack having non-recessed thin inner spacers and non-recessed thin outer spacers.

35

Figures 6 (a) - (p) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and two spacer stacks. The outermost spacer stack having recessed thin inner spacers and recessed thick outer spacers. The

inner spacer stack having recessed thin inner spacers and recessed thin outer spacers.

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DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and a device to improve
10 polycide resistance on gate electrodes less than .20 μm in width. In the following description of the several embodiments of the invention, numerous details are set forth in order to provide a thorough understanding of the present invention. It will be appreciated by one having ordinary skill in the art that the present invention may be practiced without such specific details. In other
15 instances, well known structures and techniques have not been described in detail in order to avoid obscuring the subject matter of the present invention. It will be understood by those having ordinary skill in the art that the structures of the present invention may be formed by various techniques.

20 Referring now to the drawings, one embodiment of the present invention is shown in Figures 2a - h. Figure 2a illustrates a gate layer 220 formed on a thin insulative layer 210 on a substrate 200. In one embodiment, the gate layer 220 can be a polysilicon. In one embodiment, the gate layer 220 is less than .20 μm in width. These structures are formed using conventional deposition and etching
25 techniques well-known in the art.

In Figure 2b, a thick first spacer layer 230 is deposited or grown on the gate layer 220 and substrate 200. In one embodiment, the thick first spacer layer 230 can be an oxide. In one embodiment, the thick first spacer layer 230 can be deposited or grown to a thickness in the range of approximately 200 - 600 \AA , for example, 300 \AA . It should be noted that the thick first spacer layer 230 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

30 35 In Figure 2c, a thick second spacer layer 240 is deposited or grown on the thick first spacer layer 230. In one embodiment, the thick second spacer layer 240 can be a nitride. In one embodiment, the thick second spacer layer 240 can be deposited or grown to a thickness in the range of approximately 300 - 2000 \AA , for

5 example, 800Å. It should be noted that the thick second spacer layer 240 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

10 The thick second spacer layer 240 is etched to form the spacer structure illustrated in Figure 2d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

15 The thick first spacer layer 230 is recessed by etching to form the spacer structure illustrated in Figure 2e. The recessing creates an open space between the thick second spacer layer 240 and the gate layer 220. In one embodiment, the thick first spacer layer 230 is etched approximately 60 nm deeper than the surface of the gate layer 220. In one embodiment, the etching forms a space approximately 200 - 600Å, for example, 300Å, between the thick second spacer 20 layer 240 and the gate layer 220. In one embodiment this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches. It should be noted that the side walls of the gate layer 220 are now exposed creating a larger contact (reaction) surface area.

25 In Figure 2f, a reactant layer 250 is deposited, for example by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 250 can be a metal, such as titanium.

30 The reactant layer 250 and the gate layer 220 are then annealed to form a conductive layer 260 as shown in Figure 2g. In one embodiment, the formed conductive layer 260 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be 35 performed to decrease the resistance of the conductive layer 260. It is to be noted that the conductive layer 260 can now extend beyond the edges of the gate layer 220 and is not constrained and stressed by the thick first spacer layer 230.

The unreacted portion of reactant layer 250 is etched away leaving the conductive layer 260 as illustrated in Figure 2h. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 3 a - i. Figure 3a illustrates a gate layer 320 formed on a thin insulative layer 310 on a substrate 300. In one embodiment, the gate layer 320 can be a polysilicon. In one embodiment, the gate layer 320 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 3b, a thin first spacer layer 330 is deposited or grown on the gate layer 320 and substrate 300. In one embodiment, the thin first spacer layer 330 can be an oxide. In one embodiment, the thin first spacer layer 330 is deposited or grown to a thickness in the range of approximately 50 - 300 \AA , for example, 100 \AA . It should be noted that the thin first spacer layer 330 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 3c, a thick second spacer layer 340 is deposited or grown on the thin first spacer layer 330. In one embodiment, the thick second spacer layer 340 can be a nitride. In one embodiment, the thick second spacer layer 340 is deposited or grown to a thickness in the range of approximately 300 - 2000 \AA , for example, 800 \AA . It should be noted that the thick second spacer layer 340 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 340 is etched a first time to form the structure illustrated in Figure 3d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

5 The thick second spacer layer 340 is then recessed by etching a second time to form the spacer structure illustrated in Figure 3e. In one embodiment, the thick second spacer layer 340 is etched approximately 60 nm deeper than the surface level of the gate layer 320. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of
10 isotropic etches are a wet or dry etch.

The thin first spacer layer 330 is then recessed by etching to form the spacer structure illustrated in Figure 3f. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride.
15 Examples of isotropic etches are a dry, wet or chemical bath etch. It should further be noted that the side walls of the gate layer 320 are now exposed creating a larger contact (reaction) surface area

In Figure 3g, a reactant layer 350 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 350 can be a metal, such as titanium.
20

The reactant layer 350 and the gate layer 320 are then annealed to form a conductive layer 360 as shown in Figure 3h. In one embodiment, the formed conductive layer 360 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 360. It is to be noted that the conductive layer 360 can now extend beyond the edges of the gate layer
25 320 and is not constrained and stressed.
30

The unreacted portion of reactant layer 350 is etched away leaving the conductive layer 360 as illustrated in Figure 3i. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium
35 salicide.

5 Another embodiment of the present invention is illustrated in Figures 4 a -
i. Figure 4a illustrates a gate layer 420 formed on a thin insulative layer 410 on a
silicon substrate 400. In one embodiment, the gate layer 420 can be polysilicon.
In one embodiment, the gate layer 420 is less than .20 μm in width. These
structures are formed using conventional deposition and etching techniques
10 well-known in the art.

In Figure 4b, a thin first spacer layer 430 is deposited or grown on the gate
layer 420 and substrate 400. In one embodiment, the thin first spacer layer 430
can be an oxide. In one embodiment, the thin first spacer layer 430 is deposited
15 or grown to a thickness in the range of approximately 50 - 300 \AA , for example,
100 \AA . It should be noted that the thin first spacer layer 430 can be deposited or
grown using deposition techniques that are well known in the art and are not
described in detail herein.

20 In Figure 4c, a thick second spacer layer 440 is deposited or grown on the
thin first spacer layer 430. In one embodiment, the thick second spacer layer 440
can be a nitride. In one embodiment, the thick second spacer layer 440 can be
deposited or grown to a thickness in the range of approximately 300 - 2000 \AA , for
example, 800 \AA . It should be noted that the thick second spacer layer 440 can be
25 deposited or grown using deposition techniques that are well known in the art
and are not described in detail herein.

The thick second spacer layer 440 is etched a first time to form the
structure illustrated in Figure 4d. In one embodiment, this etch is an anisotropic
30 (directional) etch which will remove nitride, but not oxide. Examples of
anisotropic etches are a dry etch or a plasma etch.

The thick second spacer layer 440 is then partially recessed by etching a
second time to form the spacer structure illustrated in Figure 4e. In one
35 embodiment, the partial recess creates a thin second spacer wall 470 adjacent to
the thin first spacer layer 430. In one embodiment, the thin second spacer wall
470 can be in the range of approximately 50 - 200 \AA , for example, 100 \AA , in width

5 and can extend approximately 60 nm deeper than the surface level of the gate layer 420. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

10 Following the partial recessing of the thick second spacer layer 440, the thin first spacer layer 430 is etched to form the spacer structure illustrated in Figure 4f. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch.

15 In Figure 4g, a reactant layer 450 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 450 can be a metal, such as titanium.

20 The reactant layer 450 and the gate layer 420 are then annealed to form a conductive layer 460 as shown in Figure 4h. In one embodiment, the conductive layer 460 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 460. It is to be noted that the conductive layer 460 can now extend beyond the edges of the gate layer 420 due to flexibility in the thin spacer walls formed from the thin first spacer layer 430 and the thin second spacer walls 470.

25 30 The unreacted portion of reactant layer 450 is etched away leaving the conductive layer 460 as illustrated in Figure 4i. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

35 Another embodiment of the present invention is illustrated in Figures 5 a - m. Figure 5a illustrates a gate layer 520 formed on a thin insulative layer 510 on a substrate 500. In one embodiment, the gate layer 520 can be polysilicon. In one

5 embodiment, the polysilicon gate layer 520 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 5b, a thin first spacer layer 530 is deposited or grown on the gate
10 layer 520 and substrate 500. In one embodiment, the thin first spacer layer 530 can be an oxide. In one embodiment, the thin first spacer layer 530 is deposited or grown to a thickness in the range of approximately 50 - 150 \AA , for example, 50 \AA . It should be noted that the thin first spacer layer 530 can be deposited or
15 grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 5c, a thin second spacer layer 540 is deposited or grown on the thin first spacer layer 530. In one embodiment, the thin second spacer layer 540 can be a nitride. In one embodiment, the thin second spacer layer 540 can be deposited or grown to a thickness in the range of approximately 50 - 150 \AA , for example, 50 \AA . It should be noted that the thin second spacer layer 540 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.
20

25 The thin second spacer layer 540 is etched a first time to form the structure illustrated in Figure 5d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

30 Following the etch of the thin second spacer layer 540, the thin first spacer layer 530 is etched to form the structure illustrated in Figure 5e. In one embodiment, this etch is an isotropic (multidirectional) which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches. It should be further noted that at this point in a process flow, implants of dopants can be
35 added to the structure to enhance circuit performance.

5 In Figure 5f, a thin third spacer layer 550 is deposited or grown. In one embodiment, the thin third spacer layer 550 can be an oxide. In one embodiment, the thin third spacer layer 550 is deposited or grown to a thickness in the range of approximately 50 -300Å, for example, 100Å. It should be noted
10 that the thin third spacer layer 550 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 5g, a thick fourth spacer layer 560 is deposited or grown on the thin third spacer layer 550. In one embodiment, the thick fourth spacer layer 560 can be a nitride. In one embodiment, the thick fourth spacer layer 560 is
15 deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick fourth spacer layer 560 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

20 The thick fourth spacer layer 560 is etched a first time to form the structure illustrated in Figure 5h. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

25 The thick fourth spacer layer 560 is then recessed by etching a second time to form the spacer structure illustrated in Figure 5i. In one embodiment, the thick fourth spacer layer 560 is etched approximately 60 nm deeper than the surface level of the gate layer 520. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of
30 isotropic etches are wet or dry etches.

The thin third spacer layer 550 is then recessed by etching to form the spacer structure illustrated in Figure 5j. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride.
35 Examples of isotropic etches are a dry, wet or chemical bath etch.

5 In Figure 5k, a reactant layer 570 is deposited, for example, by sputter,
electron beam evaporation, chemical vapor, or plasma deposition. In one
embodiment, the reactant layer 570 can be a metal such as titanium.

a
10 The reactant layer 570 and the gate layer 520 are then annealed to form a
conductive layer 580 as shown in Figure 5l. In one embodiment, the conductive
layer 580 can be a polycide, such as titanium salicide. In one embodiment, the
anneal may be performed using a rapid thermal annealing process in a nitrogen
ambient. In one embodiment, additional anneals can be performed to decrease
the resistance of the conductive layer 580. It is to be noted that the conductive
15 layer 580 can now extend beyond the edges of the gate layer 520 due to flexibility
in the thin spacer walls formed from the thin first spacer layer 530 and the thin
second spacer layer 540.

20 The unreacted reactant layer 570 is etched away leaving the conductive
layer 580 as illustrated in Figure 5m. In one embodiment, this etch is an isotropic
etch which will remove unreacted titanium, but not titanium salicide.

25 Another embodiment of the present invention is illustrated in Figures 6 a -
p. Figure 6a illustrates a gate layer 620 formed on a thin insulative layer 610 on a
substrate 600. In one embodiment, the gate layer 620 can be polysilicon. In one
embodiment, the gate layer 620 is less than .20 μ m in width. These structures are
formed using conventional deposition and etching techniques well-known in the
art.

30 In Figure 6b, a thin first spacer layer 630 is deposited or grown on the gate
layer 620 and substrate 600. In one embodiment, the thin first spacer layer 630
can be an oxide. In one embodiment, the thin first spacer layer 630 is deposited
or grown to a thickness in the range of approximately 50 - 150 Å, for example,
50 Å. It should be noted that the thin first spacer layer 630 can be deposited or
35 grown using deposition techniques that are well known in the art and are not
described in detail herein.

5 In Figure 6c, a thin second spacer layer 640 is deposited or grown on the
thin first spacer layer 630. In one embodiment, the thin second spacer layer 640
can be a nitride. In one embodiment, the thin second spacer layer 640 can be
deposited or grown to a thickness in the range of approximately 50 - 150Å, for
example, 50Å. It should be noted that the thin second spacer layer 640 can be
10 deposited or grown using deposition techniques that are well known in the art
and are not described in detail herein.

The thin second spacer layer 640 is etched a first time to form the structure
illustrated in Figure 6d. In one embodiment, this etch is an anisotropic
15 (directional) etch which will remove nitride, but not oxide. Examples of
anisotropic etches are a dry etch or a plasma etch.

Following the etch of the thin second spacer layer 640, the thin first spacer
layer 630 is etched to form the structure illustrated in Figure 6e. In one
20 embodiment, this etch is an isotropic (multidirectional) which will attack oxide,
but not nitride. Examples of isotropic etches are a dry, wet or chemical bath
etch. It should be further noted that at this point in a process flow, implants of
dopants can be added to the structure to enhance circuit performance.

25 In Figure 6f, a thin third spacer layer 650 is deposited or grown. In one
embodiment, the thin third spacer layer 650 can be an oxide. In one
embodiment, the thin third spacer layer 650 is deposited or grown to a thickness
in the range of approximately 50 - 300Å, for example 100Å. It should be noted
30 that the thin third spacer layer 650 can be deposited or grown using deposition
techniques that are well known in the art and are not described in detail herein.

In Figure 6g, a thick fourth spacer layer 660 is deposited or grown on the
thin third spacer layer 650. In one embodiment, the thick fourth spacer layer 660
can be a nitride. In one embodiment, the thick fourth spacer layer 660 is
35 deposited or grown to a thickness in the range of approximately 300 -2000Å, for
example, 800Å. It should be noted that the thick fourth spacer layer 660 can be

5 deposited or grown using deposition techniques that are well known in the art
and are not described in detail herein.

The thick fourth spacer layer 660 is etched a first time to form the structure illustrated in Figure 6h. In one embodiment, this etch is an anisotropic
10 (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick fourth spacer layer 660 is then recessed by etching a second time to form the spacer structure illustrated in Figure 6i. In one embodiment, the
15 thick fourth spacer layer 660 is etched approximately 60 nm deeper than the surface level of the gate layer 620. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are a wet or dry etch.

20 The thin third spacer layer 650 is then recessed by etching to form the spacer structure illustrated in Figure 6j. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches.

25 At this point, further etches are still to be performed, however, the substrate 600 is left exposed. Thus, if a following etch chemistry is utilized which can remove the substrate 600, the substrate 600 will need to be protected. Thus, a protective layer, for example, an oxide layer, can be provided. The provision of a protective layer is described together with the figures that follow. Alternatively,
30 if a following etch chemistry does not remove the substrate 600, then the process can continue without the necessity of providing and removing a protective layer.

In Figure 6k, a thin protective layer 670 is deposited or grown on the substrate 600. In one embodiment, the thin protective layer 670 can be oxide. In
35 one embodiment, the thin protective layer 670 is deposited or grown to a thickness in the range of approximately 50 -300Å, for example, 50Å. In one

5 embodiment, the thin protective layer 670 can be an oxide grown by annealing a silicon substrate 600 in an oxygen ambient.

The thin second spacer layer 640 is recessed by etching to form the spacer structure illustrated in Figure 6l. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thin protective layer 670 is removed and the thin first spacer layer 630 recessed by etching a second time to form the spacer structure illustrated in 15 Figure 6m. In one embodiment, the thin first spacer layer 630 is recessed approximately 60 nm deeper than the surface level of the gate layer 620. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a wet, dry or chemical bath etch. It should be noted that the side walls of the gate layer 620 are now 20 exposed creating a larger contact (reaction) surface area.

In Figure 6n, a reactant layer 680 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 680 can be a metal, such as titanium.

25 The reactant layer 680 and the gate layer 620 are then annealed to form a conductive layer 690 as shown in Figure 6o. In one embodiment, the conductive layer 690 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen 30 ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 690. It is to be noted that the conductive layer 690 can now extend beyond the edges of the gate layer 620 and is not constrained and stressed.

35 The unreacted reactant layer 680 is etched away leaving the conductive layer 690 as illustrated in Figure 6p. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

5 Through out the specification, reference has been made to isotropic and
anisotropic etching. It should be noted that the present invention may be
performed using these etch processes interchangeably, however, such
interchanging of etch processes may cause other complications. The process
steps as defined above are the preferred manner in which to perform the present
10 invention.

15 Additionally, throughout the specification, it has been stated that the etch
processes remove only the nitride or oxide layers, however, it should be noted
that such etch processes selectively remove the nitride or oxide. In other words,
an etch to remove nitride will remove nitride at a faster rate than oxide, such that
more nitride is removed and very little oxide is removed; and, an etch to remove
oxide will remove oxide at a faster rate than nitride, such that more oxide is
removed and very little nitride is removed.

20 The above described embodiments of the method and device of the
present invention provide improved polycide resistance in polysilicon gate
widths below .20 μ m. As earlier described, conductive layers, such as the
polycide, titanium salicide, can expand during formation. Previous gate
electrode structures had spacer structures which constrained this expansion.
25 This led to a stressed conductive layer that exhibited increased resistance. The
several embodiments of the present invention, reduce the stress on the formed
conductive layer thereby improving the resistance. In some embodiments,
spacers are recessed to remove constraints on the expansion of the conductive
layer. In other embodiments, spacers are partially recessed to provide thin
30 spacer walls which flex to dissipate stress. In other embodiments, dual spacer
stacks that are recessed and partially recessed also provide dissipate or remove
stress on the conductive layer. It is this reduction in the stress by the several
embodiments of the present invention, that provides improved resistance. Also,
in several of the embodiments the side walls of the gate layer are exposed to
35 allow greater surface area. This aids in formation of the conductive layer by
providing for increased nucleation sites. By aiding in formation of the
conductive layer, process yields increase.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the 10 appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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